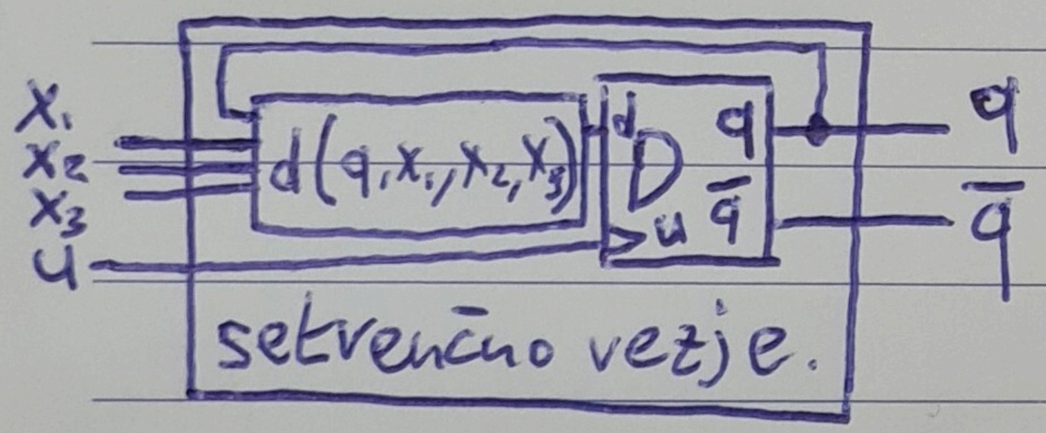
ODVDNO 8 FRI 20 23-12-24 ŠIJANEC

q	x_1	x_2	x_3	$\bar{q}$	$f_{\xi 33}$	V	D	$D^{\uparrow}q$	m
0	0	0	0	1	0	1	0	0	0
0	0	0	1	1	0	1	0	0	1
0	0	1	0	1	0	1	0	0	2
0	0	1	1	1	1	1	0	1	3
0	1	0	0	1	0	1	0	0	4
0	1	0	1	1	1	1	0	1	5
0	1	1	0	1	1	0	0	0	6
0	1	1	1	1	0	1	0	0	7
1	0	0	0	0	0	1	0	0	8
1	0	0	1	0	0	1	0	0	9
1	0	1	0	0	0	1	0	0	10
1	0	1	1	0	0	1	1	1	11
1	1	0	0	0	0	1	0	0	12
1	1	0	1	0	0	1	0	0	13
1	1	1	0	0	0	1	0	0	14
1	1	1	1	0	1	1	0	1	15

$d(q, x_1, x_2, x_3) = V(3, 5, 15)$ 11)



$d(q, x_1, x_2, x_3) =$

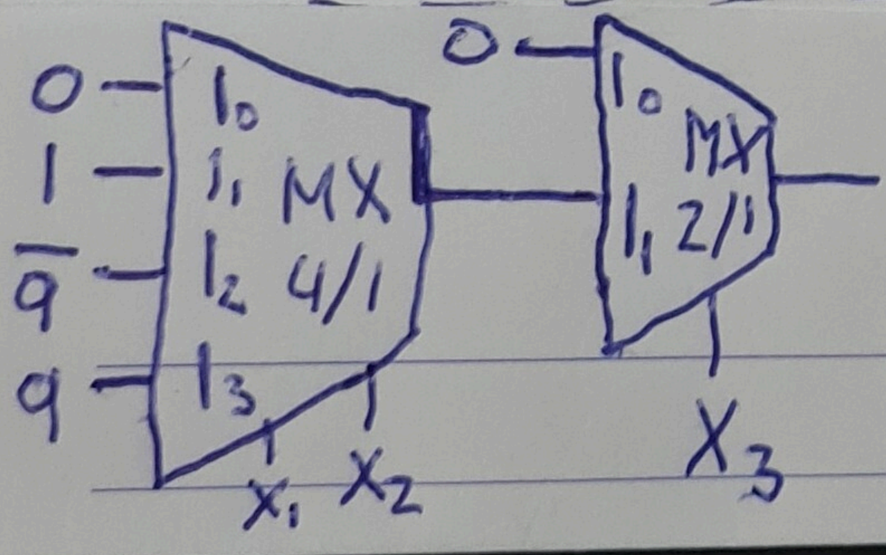
$\bar{q}\bar{x}_1 x_2 x_3 \vee \bar{q} x_1 \bar{x}_2 x_3 \vee$

$\vee q x_1 x_2 x_3 \vee q \bar{x}_1 x_2 x_3$

$= x_3(\bar{q}\bar{x}_1 x_2 \vee \bar{q} x_1 \bar{x}_2 \vee q x_1 x_2 \vee$

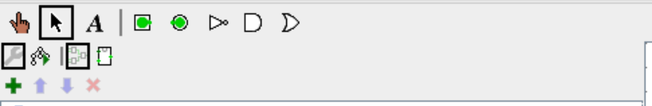
$\vee q \bar{x}_1 \bar{x}_2)$

d:



Logisim-evolution: main of domaca_naloga_8 (v 2.13.8)

File Edit Project Simulate FPGAMenu Window Help



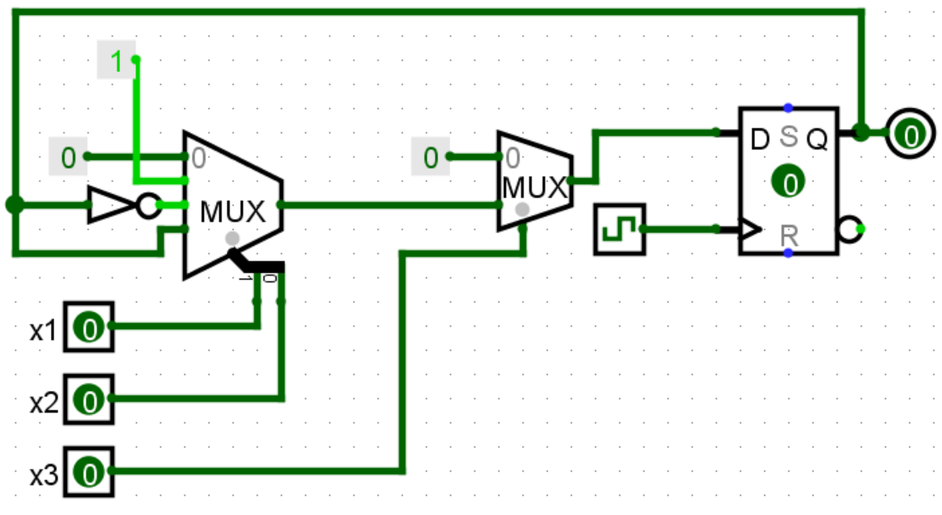
- domaca_naloga_8
  - main
  - Wiring
  - Gates
  - Plexers
  - Arithmetic
  - Memory
  - Input/Output
  - HDL-IP
  - TCL
  - Base

Properties | Registers

Circuit: main

Circuit Name	main
Shared Label	
Shared Label Facing	East
Shared Label Font	SansSerif Plain 12
Reference to VHDL architecture?	No
VHDL architecture file path	

180%



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22:48 24/12/2023